

Fault Current Limiter Optimal Placement by Harmony Search Algorithm

Saeid ZARE
TBTB.CO-Iran
aghshahed@gmail.com

AmirHossein KHAZALI
IUST.UNI-Iran
khazali@iust.ac.ir

S.Mohamad HASHEMI
TBTB.CO-Iran
modir@tbtb.co.ir

Farhad KATEBI
TBTB.CO-Iran
katebi@tbtb.co.ir

Rasol KHALILI
TBTB.CO-Iran

ABSTRACT

In this paper a harmony search algorithm has been used to determine the optimal amount and location of fault current limiters in power systems which have fault currents exceeding the permitted amount of protection equipments while using the least amount of impedance. The harmony search algorithm has been used to solve this optimization problem.

INTRODUCTION

Fault current limiters (FCL) are effective devices to overcome high fault current levels. FCLs are capable of limiting the fault current at the first peak and also limiting short circuit current at steady state without disturbing the normal operation. However in the of occurring a fault these devices increase there impedance [1].

Utilizing fault current limiters can facilitate the connection of independent power producers (IPP) to the system. It can also increase reliability of the system. However, the impedance and installation location of fault current limiters have an important effect on the mentioned, therefore developing a method that can determine the sufficient number of FCLs, there location and impedance seems to be necessary. In radial systems the appropriate place for installing fault currant limiters can be specified simply. But in loop systems this problem is complicated and requires a suitable method to determine the location, number and impedance of FCLs considering the system specifications [2].

In the few years harmony search algorithm (HSA) has been used for global optimization. HSA is a meta-heuristic algorithm which mimics the improvisation process of music players and has been developed in the recent years [4]. In this paper an optimal FCL programming is represented by harmony search algorithm. The algorithm is implemented to the IEEE 39-bus system and the results exhibit the effectiveness of the proposed method.

FAULT CURRENT CALCULATION

The majority of faults in power systems are unsymmetrical however the three phase fault is the most intensive type of faults and is used for specifying the rating of circuit breakers. In the following the calculation of fault current at each bus and the effect of three phase faults on the currents flowing in the lines are described:

Fault current at bus

For a symmetrical fault at bus i the fault current can be obtained by (1) :

$$I_i^{sc} = \frac{E_i}{Z_{ii}} \cdot I_b \quad (1)$$

Where I_i^{sc} is the fault current at bus i and E_i is the voltage before the fault at bus i which is usually assumed to be 1p.u. Z_{ii} is the diagonal members of the impedance matrix. Finally I_b is the base current. [3]

By adding the impedance Z_b between buses j and k each element of the impedance bus is modified as [3]:

$$Z_{xy}^{new} = Z_{xy}^{old} - \frac{(Z_{xj} - Z_{xk})(Z_{jy} - Z_{ky})}{Z_{jj} + Z_{kk} - 2Z_{jk} + Z_b} \quad (2)$$

Where Z_{xy}^{new} is the modified element of the impedance matrix. Therefore the effect of inserting the impedance Z_b series with the transmission line is equivalent to inserting the impedance Z_p parallel with the transmission line which can be obtained by the following relation:

$$Z_p = (-Z_b) // (Z_b + Z_{FCL}) = -\frac{Z_b(Z_b + Z_{FCL})}{Z_{FCL}} \quad (3)$$

Finally Z_p is used to modify the elements of the impedance matrix by the below relation:

$$\Delta Z_{ii} = -\frac{(Z_{ij} - Z_{ik})^2}{Z_{jj} + Z_{kk} - 2Z_{jk} + Z_p} = \frac{C_2}{C_1 + Z_p} \quad (4)$$

Hence the amount of Z_p required to reduce the fault current from $I_{i,N}$ to $I_{i,F}$ can be calculated from (5):

$$Z_p = \frac{I_{i,F}}{I_{i,N} - I_{i,F}} \frac{C_2}{Z_{ii}} - C_1 \quad (5)$$

Finally the impedance of the used fault current limiter is:

$$Z_{FCL} = -\frac{Z_b^2}{Z_b + Z_p} \quad (6)$$

Fault current Flowing through lines

During a fault in the power system if the capacity of protection equipments are not sufficient to tolerate the fault currents it can cause damages to the equipments and also interrupt the operation of the system.

Usually the analysis of fault currents is focused on there

magnitude and the magnitude of the fault current flowing from bus i to bus j caused by a fault at bus f should ($I_{i,j}^f$) not exceed the rating amounts of equipments used in the system ($|I_{i,j}^f| < |I_{spec}|$).

The fault current flowing from bus i to bus j caused by a fault at bus f can be calculated by the below equation:

$$I_{i,j}^f = \frac{(V_i - V_j - FSF_{i,j}^f V_f)}{\tilde{z}_{i,j}} \quad (7)$$

Where V_i , V_j and V_f are the voltages at buses i , j and f .

Also $FSF_{i,j}^f = (z_{i,f} - z_{j,f}) / z_{f,f}$ where $z_{a,b}$, $a, b = i, j, f$ are the elements of the impedance matrix. Also $\tilde{z}_{i,j}$ is the impedance of the line between bus i and bus j . In the normal state Z_{bus} is constant however in the case of installing new generations or fault current limiters the impedance matrix should be modified. [5]

PROBLEM FORMULATION

In this paper the goal is to reduce the fault current at each bus and the fault current flowing in lines to a specified amount. This goal is obtained by the installation of adequate fault current limiters in the system. However the total impedance used for the fault current limiters should be minimized to reduce the financial costs. Hence the problem can be formulated as following:

$$\min J_1 = \sum_{i=1}^{N_{FCL}} Z_{i,FCL}$$

s.t

$$Z_{i,FCL}^{\min} \leq Z_{i,FCL} \leq Z_{i,FCL}^{\max} \quad i = 1 \dots N_{FCL}$$

$$I_f^{sc} \leq I_j^{sc,\max} \quad f = 1 \dots B_N \quad (8)$$

$$I_{k,j}^f \leq I_{spec} \quad k, j = 1 \dots B_L$$

Where $Z_{i,FCL}$ is the impedance of the i th fault current limiter, N_{FCL} is the number of installed FCLs, $Z_{i,FCL}^{\min}$ and $Z_{i,FCL}^{\max}$ are the minimum and maximum permitted impedance of the fault current limiters. Also I_f^{sc} and $I_f^{sc,\max}$ are the fault current at bus f and the maximum specified fault current of bus f . B_N is the number of buses. Finally $I_{k,j}^f$ is the fault current flowing from bus k to bus j caused by a fault at bus f and I_{spec} is the maximum fault current flowing in the lines. B_L is the total number of lines in the system.

HARMONY SEARCH ALGORITHM

The procedure of this algorithm is in the stages are as following [15]:

1. Selecting the problem and algorithm parameters.
2. Generating harmony memory.
3. Generating a new harmony (solution vector).
4. Changing the harmony memory.
5. Terminating criteria.

Selecting the problem and algorithm parameters

In the first stage the problem is specified as following:

$$\begin{aligned} \min f(x) \\ g(x) > 0 \\ h(x) = 0 \end{aligned} \quad (9)$$

Where $f(x)$ is the object function, $g(x)$ is the inequality constraint and $h(x)$ is the equality constraint function. x is the set of each decision variable. The amount of x is restricted to $x_{L_i} \leq x_i \leq x_{U_i}$, where x_{L_i} and x_{U_i} are the lower and upper limits for each variable. Parameters of the algorithm such as harmony memory size (HMS) that is the number of solutions stored in a memory matrix, pitch adjusting rate (PAR) and the number of improvisations (iterations) are selected in this stage. Also the numbers of control variables are chosen in this step. The harmony memory (HM) is a matrix composed of control variables which each row represents a solution to the problem.

Generating harmony memory

In this stage solution vectors for the problem are generated randomly and placed in the rows of the harmony memory matrix.

$$HM = \begin{bmatrix} x_1^1 & \dots & x_N^1 \\ \vdots & \vdots & \vdots \\ x_1^{HMS} & \dots & x_N^{HMS} \end{bmatrix} \quad (10)$$

Generating a new harmony (solution vector)

When a new control variable is going to be generated for the new solution vector according to the first rule variable (x'_1) is selected from the column of the control variable and from a random row in the range of $x_1^1 - x_1^{HMS}$ from the memory matrix. The other control variables are generated in the same way. In the first stage the HMCR parameter is defined which is between 0 and 1. For the memory consideration rule a random number is generated. If this number is smaller than the HMCR parameter the control variable is selected from the memory matrix. Otherwise it is generated random in the specified range and the generation step for this control variable is terminated [4].

$$x'_1 = \begin{cases} x_1^i \in \{x_1^1, x_1^2, \dots, x_1^{HMS}\} & \text{with probability HMCR} \\ x_1^i \in X_1 & \text{with probability } 1 - \text{HMCR} \end{cases} \quad (11)$$

If the control variable is selected from memory matrix the second rule is implemented. In this step a random number is generated and if this number is smaller than the PAR

parameter which is defined in the first stage, the control variable is pitch adjusted. The pitch adjust criteria is as following [4]:

$$\text{Pitch adjusting decision for } x'_i = \begin{cases} \text{Yes} & \text{with probability PAR} \\ \text{No} & \text{with probability } 1 - \text{PAR} \end{cases}$$

If the value is 1-PAR that indicates that additional operations are unnecessary. Otherwise (x'_i) is replaced as following:

$$x'_i = x'_i \pm \text{rand} \cdot bw \quad (12)$$

In the above equation, rand is a random number between 0 and 1 and bw determines the bandwidth of the variations. In the next step regarding HM, adjusting pitch or selecting random is implemented to each control variable of the solution vector.

Changing the harmony memory

In this stage if the objective function of the new generated solution vector is better than the worst solution vector of the memory matrix the worst vector is replaced by the new generated solution vector.

Check stopping criteria

While the stopping criteria are not met the algorithm goes to step 3 and the procedure continues.

HSA FOR FCL PLACEMENT

The implementation of the proposed algorithm for the FCL placement problem includes finding the optimal value of fault current limiters and their location to restrict the fault current of buses and fault current flowing in the lines to a specified amount by using the least amount of impedance. The implementation process of HSA to the FCL placement problem is described as the following steps:

1. Generate solution vectors and place them in the HM matrix. The solution vectors consist of control variables such as the location of fault current limiters and their impedance which are in the specified range.
2. For each solution evaluate the fault currents for each solution vector.
3. Improve a new harmony (a new solution including locations and impedances). Evaluate the object function for the new harmony.
4. Compare the new harmony with the worst harmony in the HM matrix. If it is better replace the vector of the worst harmony with the new one.
5. If the stopping criteria is met find the best solution vector in the HM matrix, otherwise go to step 3.

RESULTS AND DISCUSSION

The proposed method is implemented to the IEEE 39 bus system [16]. This system consists of 39 buses and 46 lines. To start the optimization procedure initially fault currents have been calculated at each bus (assuming a symmetrical fault). Also the fault currents flowing through the lines caused by faults at other buses are also calculated. For this system the fault currents generated by symmetrical faults exceed the determined limit (20 p.u) for the following buses:

- Bus 31 with the fault current 21.8 p.u
- Bus 32 with the fault current 20.53 p.u
- Bus 33 with the the fault current 23.07 p.u
- Bus 34 with the fault current 38.14 p.u
- Bus 36 with the fault current 25.02 p.u
- Bus 38 with the fault current 26.61 p.u

Also for the below cases the fault current flowing in the lines is more than the permitted current (2p.u):

- Fault current at line 1 caused by a fault at bus 1 (4.0954 p.u)
- Fault current at line 3 caused by a fault at bus 2 (2.3612 p.u)
- Fault current at line 1 caused by a fault at bus 9 (2.0621 p.u)
- Fault current at line 3 caused by a fault at bus 25 (2.9051 p.u)
- Fault current at line 3 caused by a fault at bus 30 (2.0615 p.u)
- Fault current at line 9 caused by a fault at bus 31 (2.1332 p.u)
- Fault current at line 1 caused by a fault at bus 34 (2.1332 p.u)
- Fault current at line 3 caused by a fault at bus 34 (2.3289 p.u)
- Fault current at line 46 caused by a fault at bus 34 (2.1951 p.u)
- Fault current at line 3 caused by a fault at bus 37 (2.8807 p.u)
- Fault current at line 1 caused by a fault at bus 38 (2.4760 p.u)
- Fault current at line 1 caused by a fault at bus 39 (3.1665 p.u)

Hence six buses exist that according to the impedance of the system exceed the determined limit of fault currents. Also in twelve cases the fault current flowing in lines is more than the specified limit. So the fault current limiters should be sized and placed to have the minimum impedance (for economical concerns) in addition of limiting the fault current to the allowed limit.

The optimization problem is solved in three cases. In the first case only the fault current of the buses are reduced to the allowable limit by placing fault current limiters. In the second case the amount and location of fault current limiters are determined in the way to restrict the fault current

flowing in lines to the permitted limit. Finally in the third case the programming of fault current limiters is implemented to the system considering both type of fault currents.

For the first case the below programming has been obtained by the harmony search algorithm:

- A fault current limiter with an impedance 0.0028 p.u should be placed at line 19.
- A fault current limiter with an impedance 0.0117 p.u should be placed at line 1.
- A fault current limiter with an impedance 0.0031 p.u should be placed at line 45.
- A fault current limiter with an impedance 0.0279 p.u should be placed at line 46.

It is observed that in the case the total impedance that should be installed in the system is 0.0455 p.u.

Also it should be noticed that for the optimization problem it was defined to use four fault current limiters. In the case of using three fault current limiters the results are:

- A fault current limiter with an impedance 0.023 p.u should be placed at line 19.
- A fault current limiter with an impedance 0.0381 p.u should be placed at line 12.
- A fault current limiter with an impedance 0.1 p.u should be placed at line 46.

It is observable that in this case the total impedance used for the system is 0.1404 p.u. specifying the number of fault current limiters used for the system depends on the costs on installation, operation and other economical aspects that unfortunately are not available and therefore determining the number of fault current limiters is not possible. It should be mentioned that it is not possible to reduce the fault current at buses to below the determined limits by using only two fault current limiters(considering the defined range for there impedance).

In the second case the fault current limiters are used to restrict the fault current flowing in the lines to a acceptable level. The following results are acquired after solving the optimization problem by harmony search algorithm:

- A fault current limiter with an impedance 0.0083 p.u should be placed at line 46.
- A fault current limiter with an impedance 0.0095 p.u should be placed at line 3.
- A fault current limiter with an impedance 0.00423 p.u should be placed at line 46.
- A fault current limiter with an impedance 0.095 p.u should be placed at line 11.
- A fault current limiter with an impedance 0.0043 p.u should be placed at line 1.

In this case the total impedance that should be installed in the system is 0.1213 p.u. The optimization problem was defined to use four fault current limiters. In the case of using three fault current limiters the results are:

- A fault current limiter with an impedance 0.065

p.u should be placed at line 3.

- A fault current limiter with an impedance 0.0941 p.u should be placed at line 46.
- A fault current limiter with an impedance 0.076 p.u should be placed at line 1.

Also in this case using two fault current limiters is not adequate for restricting the fault current.

In the last case both type of fault currents are restricted. For this case at least four fault current limiters should be used to decrease the fault current at each bus to under 20 p.u and the fault current flowing in lines to under 2 p.u. The results attained for this case is:

- A fault current limiter with an impedance 0.0105 p.u should be placed at line 19.
- A fault current limiter with an impedance 0.4194 p.u should be placed at line 1.
- A fault current limiter with an impedance 0.020 p.u should be placed at line 41.
- A fault current limiter with an impedance 0.0034 p.u should be placed at line 30.

CONCLUSION

In this paper an FCL sizing and placement scheme is presented. The fault current limiters are placed with the goal to restrict the fault currents at buses and the fault currents flowing through lines caused by faults at other buses. In this paper to the optimization problem is defined in order to minimize the used impedance while satisfying the defined constraints. The proposed method is implemented to the 39 bus IEEE system and harmony search algorithm is used to solve the optimization problem. The results show that the fault currents are suppressed to the admissible levels using the least impedance.

REFERENCES

- [1] M. Noe, , 1999 "Technical and economical benefits of superconducting fault current limiters in power systems," IEEE Trans. On Applied Superconductivity, vol. 9, no. 2, pp. 1347–1350.
- [2] Fault Current Limiter Technical Committee, , Technical Report of the IEE of Japan, no. 709, 1999.
- [3] J. H. Teng, 2010 " Optimum fault current limiter placement with search space reduction technique" IET Gener. Transm. Distrib., Vol. 4, Iss. 4, pp. 485–494
- [4] Z. W. Geem, 2001 "A new heuristic optimization algorithm : harmony search, Simulation 76 (2) 60-68
- [5] M.Mahdavi, 2007 "An improved harmony search algorithm for solving optimization problems" Applied mathematics and computation 188(2):1567–79.